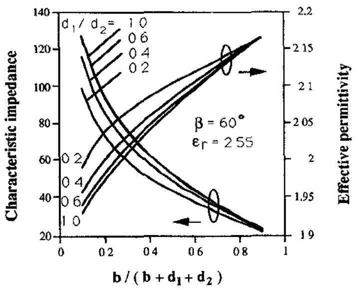

Fig. 5. Variation of Z_0 and ε_{eff} as a function of shape ratio taking d_1/d_2 as a parameter for VSML, $W = b + d_1 + d_2, \beta = 60°$.

an increase of its relative effective dielectric constant. However, these variations are not significant for small asymmetry and large shape ratio. For a given shape ratio and asymmetrical factor (d_1/d_2), the impedance is higher with lower value of β. This is simply because of the decreasing separation between the center conductor and the ground plane. Note that due to the many available parameters in design, a wide range of impedances may therefore be obtained.

VI. Conclusion

Two sets of simple, explicit formulas have been developed for the evaluation of the quasi-TEM characteristic parameters of asymmetrical V-shaped microshield line. The numerical accuracy of these expressions is verified by comparing the results with the ones obtained by a standard numerical technique. It has been observed that the accuracy of the new set of formulas are good enough in many practical situations. Higher accuracy may further be achieved, in a step by step manner, by increasing the order of the model in representating the original integral. The numerical results show that the characteristic impedance and relative effective permittivity of VSML vary slowly with the onset of asymmetry.

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Nonlinear Yield Analysis and Optimization of Monolithic Microwave Integrated Circuits

Stefano D'Agostino and Claudio Paoloni

***Abstract*—In this paper, a discussion about nonlinear yield evaluation and nonlinear yield optimization of MMIC circuits using a physics-based nonlinear lumped-element MESFET model is presented. The lumped elements of the MESFET model are directly calculated by closed expressions related to process parameters. One of the main features of the model is the easy and effective implementation in commercial CAD tools. It allows the use of nonlinear yield algorithms assuming, as statistical variables, the parameters of the technological process, such as: doping density, gate channel length, etc., maintaining at the same time, the advantages of lumped-element MESFET model, in particular fast computation and reduction of convergence problems in harmonic balance for complex circuit topologies.**

I. Introduction

MMIC technology, due to the extremely limited postprocessing tuning facility, requires an accurate prediction of the manufacturing yield of circuit and an effective procedure to improve the yield if not adequate. Many contributions regard yield analysis as well as yield optimization were presented in literature [1]–[6].

Typically a MMIC circuit is composed by active and passive components on the same substrate. Both components contribute to circuit yield. Passive elements are mainly sensible to geometrical variations and to the substrate parameters as effective dielectric constant ϵ_r and height h, while the active elements are also sensible to process variations.

To effectively evaluate the yield of the circuit, and eventually improve it, the use of models of circuit elements accurately related to the MMIC process parameters, to account for variations of the electrical behavior caused by the variations in the process parameters is mandatory. Especially if technological process is well established and allows high performance circuits, an accurate yield evaluation and yield optimization bring forth relevant advantages by finely controlling the process parameters around their nominal values.

Two approaches for yield analysis, from the circuit point of view, can be distinguished. The first one is based on the use of lumped-element model of active devices for both small signal and large signal cases. The yield analysis is performed varying statistically the values of the linear and nonlinear lumped elements composing the model such as capacitors, inductors, resistors, and nonlinear components. The advantage of this approach consists in the immediate implementation of the active device model in commercial CAD tools that usually contain Monte Carlo analysis algorithms. The computational time to obtain the final result is very short. The drawback of the approach consists in the lack of any direct relationship with process parameters and even if the result of yield analysis can be indicative, a following yield optimization is hardly applicable to the technological process.

The second approach is based on circuit models of active devices related to process parameters. The yield analysis performed by this approach is very accurate and is directly linked to the parameters of

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S. D'Agostino is with the University of Roma La Sapienza, Department of Electronic Engineering, 00184, Rome, Italy.

C. Paoloni is with the University of Roma Tor Vergata, Department of Electrical Engineering, 00133, Rome, Italy.

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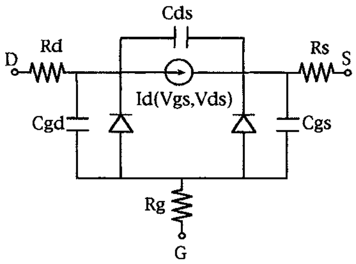

Fig. 1. Large signal Statz-Pucel MESFET model.

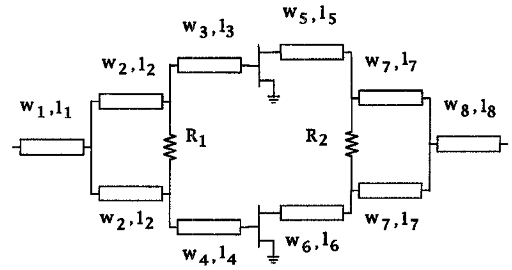

Fig. 2. Schematic of the investigated amplifier.

the process. The results of the yield optimization can be effectively applicable to the technological process to improve the final yield of the circuit. The drawbacks of this approach consist in the high analytical complexity of the models, in the long computational time, especially in nonlinear case, in convergence problem of harmonic balance simulations and hard implementation of the model in commercial CAD tools. Usually stand-alone computer programs using these kinds of models, based on the process parameters, must be developed.

The purpose of this paper is to discuss nonlinear yield analysis and optimization of MMIC circuits performed by using a large-signal MESFET model composed of lumped elements calculated by close expressions related to the process parameters. Such a "family" of models unifies the advantages of both lumped-element models, based on semiempirical parameters, and physical models, based on process parameters. Furthermore, the process parameters are assumed as statistical variables in the proposed active devices models allowing a clear understanding of the yield analysis result and the implementation of the values of the statistical variables, obtained from the yield optimization, in the technological process. The use of such a "family" of models is demonstrated to be effective in nonlinear yield analysis and optimization, typically very complex and time consuming. The nonlinear MESFET model presented in [7], [8] belonging to the "family" of model based on lumped elements, whose values are directly related to the process parameters, is adopted in the following.

In Section II the large-signal MESFET model is introduced. In Section III a circuit example of nonlinear yield analysis and optimization is described as test vehicle. Some considerations on yield optimization criteria are also discussed.

II. The MESFET Model

Recently, the problem of interaction between physical model of GaAs MESFET's and simulation programs, based on an equivalent circuit, has stimulated a considerable interest. As a matter of fact, in MMIC technology, getting simple and immediate expressions showing the relations between the elements of the equivalent circuit and the physical-geometrical characteristics of the device is of great importance, both for good circuit design and for the subsequent optimization steps. This is especially true if the circuit consists of a large number of devices.

The "empirical" I_d expression of Statz-Pucel model is [9] (Fig. 1)

$$I_d(V_{gs}, V_{ds}) = \frac{\beta(V_{gs} - V_T)^2}{1 + b(V_{gs} - V_t)} P(\alpha, V_{ds})(1 + \lambda V_{ds}) \quad (1)$$

where

$$P(\alpha, V_{ds}) = \begin{cases} 1 - \left(1 - \alpha\frac{V_{ds}}{3}\right)^3 & \text{for } 0 < V_{ds} < 3/\alpha \\ 1 & \text{for } V_{ds} \geq 3/\alpha. \end{cases} \quad (2)$$

The first factor in (1) represents the current in full saturation. This value is the limit above which, if the term $(1+\lambda V_{ds})$ is neglected, the drain current does not further increase, when the condition $V_{ds} > 3/\alpha$ is realized.

Simple physics-based expressions for the empirical parameters b, β, α, and λ were found in [7].

The physics-based expressions for the empirical parameters C_{gso} and C_{gdo} of the MESFET equivalent circuit capacitances $C_{gs}(V_{gs}, V_{ds})$, $C_{gd}(V_{gd}, V_{ds})$ were also obtained in [8].

The presented physics-based equations were included, in a microwave simulator [10], making available, for the MMIC design, the physical and geometrical parameters of the foundry process.

III. Yield Analysis and Optimization of Large Signal MMIC

In this section an application of nonlinear yield analysis and optimization is presented adopting the large-signal lumped-element MESFET model based on process parameters introduced in Section II.

A typical two-MESFET large-signal amplifier (Fig. 2) was investigated. The active devices adopted in the design, 1 μm gate length, are referenced in [11], where all the process parameters were extensively supplied, to be included in the nonlinear MESFET model of Section II. Of course, the performance of the designed amplifier is meaningful in the following discussion on the yield analysis.

The amplifier was biased with $V_{dd} = 5$ V and $V_{gg} = -0.8$. The bandwidth was chosen in the range 3.1–4.3 GHz with a required nominal output power of 7.5+/−1 dB at 0 dBm of input power. The substrate parameters are common both to passive and active elements. Since the two MESFET's are physically located adjacent on the substrate the same statistical variations can be reasonably assumed. All the analysis and optimizations were performed by using LIBRA$^{(TM)}$ simulator, a commercial microwave CAD tool.

The statistical variables included in the circuit were 29. Eighteen statistical variables for the passive elements, in particular length l_i and width w_i of the i-th microstrip line and the values of isolation resistors of the input (R_1) and output (R_2) Wilkinson combiners. Eleven statistical variables for technological parameters: dielectric constant ϵ_r, height of the substrate h, gate width Z, gate length L, doping density of the active zone N_D, built-in voltage of Schottky contact V_{bi}, domain parameter K_d, gate resistor R_g, source resistor R_s, electric field value at the electron drift velocity saturation E_s, and active-layer thickness a. According to the typical characteristics of GaAs foundry process [12] statistical Gaussian distribution of the variables was chosen and the standard deviation is shown in Table I. The correlation among the statistical process variables was neglected.

Some considerations must be introduced about the criteria of yield optimization used in this paper. The purpose of the yield optimization is to determine proper values of the statistical variables to be applied in the technological process to improve the yield of the circuit before optimization. Unfortunately, not all the statistical variables are controllable in the process, but, of course, the result of the yield after optimization is dependent also from the uncontrollable statistical

TABLE I

Statistical variables	Deviation (%)
l_i . length of i-th microstrip line	3
w_i :width of i-th microstrip line	3
R_1, R_2	3
ε_r	1.5
h	0.02
Z	5
L	5
N_D	5
V_{bi}	5
K_d	2.5
E_s	5
a	5
R_g	2.5
R_s	2.5

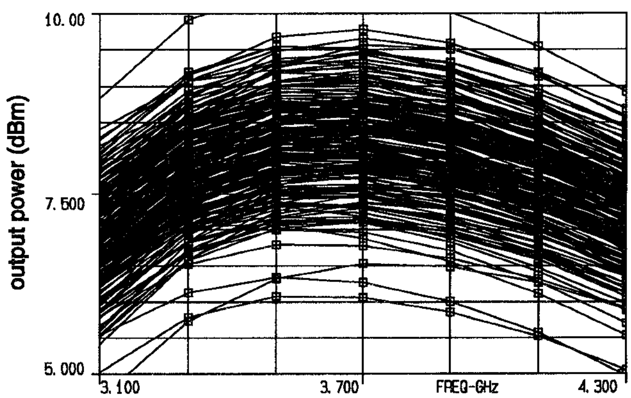

Fig. 3. Statistical variation of output power versus frequency before yield optimization.

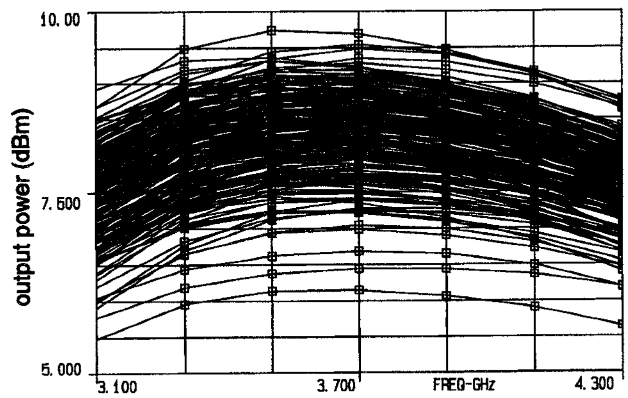

Fig. 4. Statistical variation of output power versus frequency after yield optimization.

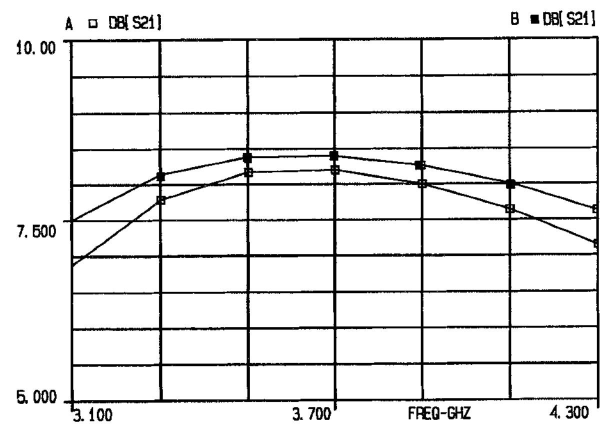

Fig. 5. Small signal gain before (B) and after (A) yield optimization.

variables of the technological process. To correctly perform the yield optimization, only the controllable statistical variables (active-layer thickness a, gate width Z, gate length L, doping density of the active zone N_D, height of the substrate h, length l_i and width w_i of the i-th microstrip line, and the values of isolation resistors of the input (R_1) and output (R_2) Wilkinson combiners) can be used, maintaining at the same time, the uncontrollable statistical variables (built-in voltage of Schottky contact V_{bi}, dielectric constant ϵ_r, domain parameter K_d, gate resistor R_g, source resistor R_s, electric field value at the electron drift velocity saturation E_s) fixed at their nominal values. After the yield optimization phase, the yield analysis was again performed allowing the statistical variables, controllable and uncontrollable, to vary in their appropriate statistical range (Table I). Of course, adopting this procedure the yield analysis of the optimized circuit will not be so optimistic as in the conventional procedure where only the controllable statistical variables were considered.

The nonlinear yield analysis, for the circuit before yield optimization, was performed assuming as a goal the output power constrained in the range of 7–9 dBm at 0 dBm of input power, in the whole frequency range. A yield of 23.8% was achieved.

A nonlinear yield optimization was then performed. The above described procedure was now applied to the circuit example. Yield optimization was performed considering only the controllable statistical variables. Then two different yield analyses of the resulting circuit were performed. First, the yield of the circuit was computed including only the controllable variable, then both controllable and uncontrollable statistical variables were considered. In the first case, where only the controllable variables are considered, a yield of 67.8% was obtained. Introducing in the yield analysis also the uncontrollable statistical variables the final yield of 60.6% was obtained. Both yield analysis values were obtained after 1 000 iteration steps by using Monte Carlo statistical algorithm for the nonlinear yield analysis of the circuit. Consequently neglecting the effect of the uncontrollable statistical variables causes a significant error in yield evaluation.

Another significant advantage of the introduction in yield procedure of the nonlinear lumped-element MESFET model based on process parameter [7], [8] consists in the drastically reduction of CPU time. In fact, the presented yield optimization was performed in 50 minutes of CPU time (workstation IBM RISC 6 000/320), that is a remarkable result considering the nonlinear nature of the computation.

The statistical variations of the output power, for an input power of 0 dBm, are shown in Fig. 3 for the circuit before yield optimization and in Fig. 4 for the circuit after yield optimization. The S-parameters of the circuit before yield optimization and of the circuit after yield optimization are compared in Fig. 5 (gain) and in Fig. 6 (input reflection coefficient, S_{11}). Although a nonlinear yield optimization was performed, a remarkable improvement of S-parameters was also obtained.

IV. Conclusion

A fast and effective procedure for nonlinear yield analysis and optimization based on a large-signal lumped-element MESFET model related to the MMIC process parameters has been presented. A typical large-signal amplifier has been designed and investigated from the point of view of nonlinear yield performance. The opportunity of introducing the MMIC process parameters in the yield analysis, performed by using commercial CAD tools, allows, at the same time,

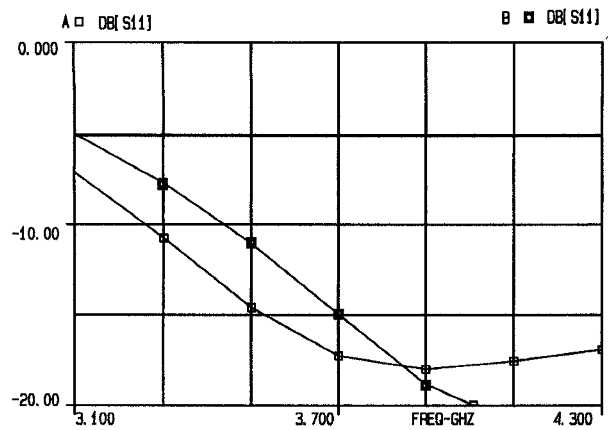

Fig. 6. Input reflection coefficient before (B) and after (A) yield optimization.

to achieve the advantages of physic-based model maintaining the features of lumped-element MESFET model.

The advantages of performing nonlinear yield analysis adopting such a kind of MESFET model demonstrate the importance to devote further efforts in the derivation of new and accurate large-signal model based on lumped elements directly related, by closed expressions, to the MMIC process parameters.

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28 GHz Omni-Directional Quasi-Optical Transmitter Array

Mark J. Vaughan and Richard C. Compton

Abstract—**Omni-directional base stations are needed in many emerging wireless communication systems. This paper presents the first adaptation of a quasi-optical oscillator array for this purpose. A 28 GHz active oscillator element containing a modified Vivaldi endfire antenna is utilized as the unit cell. Twelve of these are incorporated into the circular array, which is powered from a single dc power supply. The array has a high combining efficiency and remains frequency-locked over a span of 600 MHz.**

I. INTRODUCTION

Because of the low millimeter-wave output power available from solid-state devices, it will be necessary for many applications (aside from those where vacuum tubes are acceptable) to use a plurality of devices to generate adequate amounts of power. Quasi-optical arrays use free-space combination to efficiently sum the outputs of multiple devices [1].

To date, quasi-optical research has focused on planar arrays to replace traveling-wave tubes for point-to-point and radar applications. The printed-circuit type antennas integrated into these arrays nearly all operate broadside. These include the microstrip patches [2], [3], the grid antennas [4], slot antennas [5], [6], waveguide probes [7], and dipoles [8]. The only exceptions are antennas used with dielectric waveguide resonators [9] and the tapered slot antennas (TSA), which can be found in a variety of endfire applications [10]–[13]. However, these, like the broadside antennas, have strictly been used in active arrays for directing the output power into a single direction.

These systems are not well suited for local multipoint distribution services (LMDS) where a base station must communicate with multiple subscribers in a cellular configuration. For LMDS an omni-directional transmitter is needed, and the tapered slot antennas are ideal for this purpose. They can be arranged on a single circular planar substrate to radiate azimuthally in all directions [14]. Further, since the active circuits are all located in the center of such an array, they can be monolithically fabricated separately from the antennas. This eliminates the excessive costs of fabricating the relatively large antennas on expensive GaAs substrates. GaAs is also an undesirable antenna substrate because of its high dielectric-constant. The circular nature of the array means that the coupling lines between the elements in an oscillator array form a closed loop, which has been shown in standard rectangular arrays to have benefit in reducing the number of

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The authors are with the School of Electrical Engineering, Cornell University, Ithaca, NY 14853 USA.

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